In th Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 CFR § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.

A marked-up version showing amendments to any claims being changed in provided in one or more accompanying pages separate from this amendment in accordance with 37 CFR § 1.121(c)(1)(ii). Any claim not accompanied by a marked-up version has not been changed relative to the immediate prior version, except that marked-up versions are not being supplied for any added claim or canceled claim.

CLAIMS

1. A method of forming memory circuitry sequentially comprising:

forming a plurality of metal interconnect lines over a semiconductive substrate; and

forming a plurality of memory cell storage devices comprising voltage or current controlled resistance setable semiconductive material.

2. The method of claim 1 wherein the memory cell storage devices respectively comprise two electrodes separated by said resistance setable semiconductive material.

3. The method of claim 1 wherein the metal interconnect lines comprise a conductive elemental metal or metal alloy comprising at least two elemental metals.

4. The method of claim 1 wherein the metal interconnect lines comprise at least one conductive metal compound other than a silicide.

5. The method of claim 1 wherein the metal interconnect lines comprise a conductive metal silicide.

6. The method of claim 1 wherein the metal interconnect lines comprise both a) a conductive elemental metal or metal alloy comprising at least two elemental metals, and b) at least one conductive metal compound other than a conductive metal silicide.

B1 (continued)

7. The method of claim 1 wherein said resistance setable semiconductive material comprises chalcogenide material having metal ions diffused therein.

8. The method of claim 7 wherein the chalcogenide material having metal ions diffused therein comprises Ge_xA_y, where A is selected from the group consisting of Se, Te and S, and mixtures thereof.

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9. A method of forming memory circuitry sequentially comprising:

forming a plurality of memory cell access transistor gates over a semiconductor substrate;

forming a plurality of a metal interconnect lines over the substrate and the memory cell access transistor gates; and

forming a plurality of memory cell storage devices comprising voltage or current controlled resistance setable semiconductive material.

10. The method of claim 9 wherein said resistance setable semiconductive material comprises chalcogenide material having metal ions diffused therein.

11. The method of claim 10 wherein the chalcogenide material having metal ions diffused therein comprises Ge_xA_y, where A is selected from the group consisting of Se, Te and S, and mixtures thereof.

(continued)

12. (Amended) A method of forming random access memory circuitry comprising:

forming a plurality of memory cell access transistor gates over a semiconductor substrate;

forming a plurality of metal interconnect lines over the substrate and the memory cell access transistor gates;

after forming the conductive metal interconnect lines, forming respective first memory cell electrodes in electrical connection with respective memory cell access transistors incorporating the memory cell access transistor gates;

forming voltage or current controlled resistance setable semiconductive material in electrical connection with the respective first electrodes; and

forming at least one second memory cell electrode in electrical connection with the voltage or current controlled resistance setable material.

13. The method of claim 12 wherein said resistance setable semiconductive material comprises chalcogenide material having silver ions diffused therein.

14. The method of claim 13 wherein at least one of the first and second electrodes comprises silver.

15. The method of claim 13 wherein at least one of the first and second electrodes comprises elemental silver.

16. The method of claim 12 comprising after forming the memory cell access transistor gates and before forming the respective first memory cell electrodes, depositing a boron and/or phosphorus doped silicon dioxide glass comprising layer, and reflowing it at a temperature of at least 750°C.

B1 (continued)

17. (Amended) A method of forming at least two random access memory cells comprising:

forming at least two memory cell wordlines over a semiconductor substrate, the two memory cell wordlines being proximate one another;

forming at least one metal bit line in electrical connection with active area of the semiconductive substrate which is between the two memory cell wordlines;

after forming the metal bit line, forming respective first memory cell electrodes in electrical connection with active area of the semiconductive substrate on respective lateral outer sides of the two wordlines;

forming voltage or current controlled resistance setable semiconductive material in electrical connection with the respective first electrodes; and

forming a second memory cell electrode in electrical connection with the voltage or current controlled resistance setable material, the second memory cell electrode being common to the two memory cells being formed.

18. The method of claim 17 comprising forming the first memory cell electrodes, said resistance setable semiconductive material, and the second memory cell electrode into respective memory cell container shapes.

19. The method of claim 17 wherein said resistance setable semiconductive material comprises chalcogenide material having silver ions diffused therein.

B1 (Continued)

20. The method of claim 19 wherein at least one of the first and second electrodes comprises silver.

21. The method of claim 19 wherein at least one of the first and second electrodes comprises elemental silver.

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22. A method of forming integrated circuitry comprising:

forming a metal interconnect line over a semiconductive substrate; and

forming a device comprising two metal comprising electrodes separated by a voltage or current controlled resistance setable semiconductive material, said resistance setable semiconductive material being formed after forming the metal interconnect line.

23. The method of claim 22 wherein the metal interconnect line comprises a conductive elemental metal or metal alloy comprising at least two elemental metals.

24. The method of claim 22 wherein the metal interconnect line comprises at least one conductive metal compound other than a silicide.

25. The method of claim 22 wherein the metal interconnect line consists essentially of a conductive elemental metal or metal alloy comprising at least two elemental metals.

26. The method of claim 22 wherein the metal interconnect lines consists essentially of a conductive metal compound other than a silicide.

(Continued)

27. The method of claim 22 wherein said resistance setable semiconductive material comprises chalcogenide material having metal ions diffused therein.

28. The method of claim 27 wherein the chalcogenide material having metal ions diffused therein comprises Ge_xA_y, where A is selected from the group consisting of Se, Te and S, and mixtures thereof.

29. The method of claim 22 wherein the metal interconnect line comprises both a) a conductive elemental metal or metal alloy comprising at least two elemental metals, and b) at least one conductive metal compound other than a silicide.

30. The method of claim 22 wherein the device comprises at least a portion of a memory cell.

31. A method of forming integrated circuitry comprising:

forming at least two conductive device components over a semiconductor substrate;

forming a metal interconnect line over the two conductive device components;

forming at least one opening through the metal interconnect line to at least one of the two conductive device components; and

forming voltage or current controlled resistance setable semiconductive material within the opening in electrical connection with a respective one of the two device components and in electrical connection with the metal interconnect line.

32. The method of claim 31 wherein at least one of the device components comprises a conductive line.

33. The method of claim 31 wherein forming the opening comprises photolithography and etching of the metal interconnect line.

34. The method of claim 31 wherein said resistance setable semiconductive material comprises chalcogenide material having silver ions diffused therein.

35. The method of claim 34 wherein at least one of the device components comprises silver.

36. The method of claim 34 wherein at least one of the device components comprises elemental silver.

37. A method of forming integrated circuitry comprising:

forming at least two conductive device components over a semiconductor substrate;

forming a metal interconnect line over the two conductive device components;

forming at least one opening through the metal interconnect line to at least one of the two conductive device components;

forming voltage or current controlled resistance setable semiconductive material within the opening in electrical connection with a respective one of the two device components, said resistance setable semiconductive material being formed to only partially fill the opening; and

forming a conductive material within the opening in electrical connection with said resistance setable semiconductive material and the metal interconnect line.

38. The method of claim 37 wherein the conductive material is formed to less than completely fill remaining portions of the opening.

39. The method of claim 37 wherein the conductive material is formed to less than completely fill remaining portions of the opening, and to form a container shape.

40. The method of claim 37 wherein the conductive material comprises silver.

41. The method of claim 37 wherein the conductive material comprises elemental silver.

42. The method of claim 37 wherein said resistance setable semiconductive material comprises chalcogenide material having metal ions diffused therein.

(continued)

43. The method of claim 42 wherein the chalcogenide material having metal ions diffused therein comprises Ge_xA_y, where A is selected from the group consisting of Se, Te and S, and mixtures thereof.

44. The method of claim 37 wherein said resistance setable semiconductive material comprises chalcogenide material having silver ions diffused therein.

45. The method of claim 44 wherein the conductive material comprises silver.

46. The method of claim 44 wherein the conductive material comprises elemental silver.

Add new claims 47-88 as follows:

47. (Added) A method of forming memory circuitry sequentially comprising:

forming a plurality of metal interconnect lines over a semiconductive substrate; and

forming a plurality of memory cell storage devices comprising chalcogenide material.

48. (Added) The method of claim 47 wherein the memory cell storage devices respectively comprise two electrodes separated by said chalcogenide material.

49. (Added) The method of claim 47 wherein the metal interconnect lines comprise a conductive elemental metal or metal alloy comprising at least two elemental metals.

50. (Added) The method of claim 47 wherein the metal interconnect lines comprise at least one conductive metal compound other than a silicide.

51. (Added) The method of claim 47 wherein the metal interconnect lines comprise a conductive metal silicide.

52. (Added) The method of claim 47 wherein the metal interconnect lines comprise both a) a conductive elemental metal or metal alloy comprising at least two elemental metals, and b) at least one conductive metal compound other than a conductive metal silicide.

B1 (continued)

53. (Added) A method of forming memory circuitry sequentially comprising:

forming a plurality of memory cell access transistor gates over a semiconductor substrate;

forming a plurality of a metal interconnect lines over the substrate and the memory cell access transistor gates; and

forming a plurality of memory cell storage devices comprising chalcogenide material.

54. (Added) The method of claim 53 wherein the chalcogenide material comprises Ge_xA_y, where A is selected from the group consisting of Se, Te and S, and mixtures thereof.

55. (Added) A method of forming random access memory circuitry comprising:

forming a plurality of memory cell access transistor gates over a semiconductor substrate;

forming a plurality of metal interconnect lines over the substrate and the memory cell access transistor gates;

after forming the conductive metal interconnect lines, forming respective first memory cell electrodes in electrical connection with respective memory cell access transistors incorporating the memory cell access transistor gates;

forming chalcogenide comprising material in electrical connection with the respective first electrodes; and

forming at least one second memory cell electrode in electrical connection with the chalcogenide comprising material.

56. (Added) The method of claim 55 wherein said chalcogenide comprising material has silver ions diffused therein.

57. (Added) The method of claim 56 wherein at least one of the first and second electrodes comprises silver.

58. (Added) The method of claim 56 wherein at least one of the first and second electrodes comprises elemental silver.

59. (Added) The method of claim 55 comprising after forming the memory cell access transistor gates and before forming the respective first memory cell electrodes, depositing a boron and/or phosphorus doped silicon dioxide glass comprising layer, and reflowing it at a temperature of at least 750°C.

60. (Added) A method of forming at least two random access memory cells comprising:

forming at least two memory cell wordlines over a semiconductor substrate, the two memory cell wordlines being proximate one another;

forming at least one metal bit line in electrical connection with active area of the semiconductive substrate which is between the two memory cell wordlines;

after forming the metal bit line, forming respective first memory cell electrodes in electrical connection with active area of the semiconductive substrate on respective lateral outer sides of the two wordlines;

forming chalcogenide comprising material in electrical connection with the respective first electrodes; and

forming a second memory cell electrode in electrical connection with the chalcogenide comprising material, the second memory cell electrode being common to the two memory cells being formed.

61. (Added) The method of claim 60 comprising forming the first memory cell electrodes, said chalcogenide comprising material, and the second memory cell electrode into respective memory cell container shapes.

62. (Added) The method of claim 60 wherein said chalcogenide comprising material has silver ions diffused therein.

63. (Added) The method of claim 62 wherein at least one of the first and second electrodes comprises silver.

64. (Added) The method of claim 62 wherein at least one of the first and second electrodes comprises elemental silver.

(continued)

65. (Added) A method of forming integrated circuitry comprising:

forming a metal interconnect line over a semiconductive substrate; and

forming a device comprising two metal comprising electrodes separated by a chalcogenide comprising material, said chalcogenide comprising material being formed after forming the metal interconnect line.

66. (Added) The method of claim 65 wherein the metal interconnect line comprises a conductive elemental metal or metal alloy comprising at least two elemental metals.

67. (Added) The method of claim 65 wherein the metal interconnect line comprises at least one conductive metal compound other than a silicide.

68. (Added) The method of claim 65 wherein the metal interconnect line consists essentially of a conductive elemental metal or metal alloy comprising at least two elemental metals.

69. (Added) The method of claim 65 wherein the metal interconnect lines consists essentially of a conductive metal compound other than a silicide.

70. (Added) The method of claim 65 wherein the chalcogenide comprising material comprises Ge_xA_y, where A is selected from the group consisting of Se, Te and S, and mixtures thereof.

71. (Added) The method of claim 65 wherein the metal interconnect line comprises both a) a conductive elemental metal or metal alloy comprising at least two elemental metals, and b) at least one conductive metal compound other than a silicide.

(continued)

72. (Added) The method of claim 65 wherein the device comprises at least a portion of a memory cell.

73. (Added) A method of forming integrated circuitry comprising:

forming at least two conductive device components over a semiconductor substrate;

forming a metal interconnect line over the two conductive device components;

forming at least one opening through the metal interconnect line to at least one of the two conductive device components; and

forming chalcogenide comprising material within the opening in electrical connection with a respective one of the two device components and in electrical connection with the metal interconnect line.

74. (Added) The method of claim 73 wherein at least one of the device components comprises a conductive line.

75. (Added) The method of claim 73 wherein forming the opening comprises photolithography and etching of the metal interconnect line.

B1 (continued)

76. (Added) The method of claim 73 wherein said chalcogenide comprising material has silver ions diffused therein.

77. (Added) The method of claim 76 wherein at least one of the device components comprises silver.

78. (Added) The method of claim 76 wherein at least one of the device components comprises elemental silver.

79. (Added) A method of forming integrated circuitry comprising:

forming at least two conductive device components over a semiconductor substrate;

forming a metal interconnect line over the two conductive device components;

forming at least one opening through the metal interconnect line to at least one of the two conductive device components;

forming chalcogenide comprising material within the opening in electrical connection with a respective one of the two device components, said chalcogenide comprising being formed to only partially fill the opening; and

forming a conductive material within the opening in electrical connection with said chalcogenide comprising material and the metal interconnect line.

(continued)

80. (Added) The method of claim 79 wherein the conductive material is formed to less than completely fill remaining portions of the opening.

81. (Added) The method of claim 79 wherein the conductive material is formed to less than completely fill remaining portions of the opening, and to form a container shape.

82. (Added) The method of claim 79 wherein the conductive material comprises silver.

83. (Added) The method of claim 79 wherein the conductive material comprises elemental silver.

84. (Added) The method of claim 79 wherein said chalcogenide comprising material has metal ions diffused therein.

85. (Added) The method of claim 84 wherein the chalcogenide material having metal ions diffused therein comprises Ge_xA_y, where A is selected from the group consisting of Se, Te and S, and mixtures thereof.

B1 (concluded)

86. (Added) The method of claim 79 wherein said chalcogenide comprising material has silver ions diffused therein.

87. (Added) The method of claim 86 wherein the conductive material comprises silver.

88. (Added) The method of claim 86 wherein the conductive material comprises elemental silver.